# MODEL QUESTION PAPER - I

**Time : 3 Hrs** **Max Marks : 100**

**Note : (i) Answel all the question from Part - A. Each question carries 3 marks.**

**(ii) Answer division (A) or (B) of each question in Part - B. Each question carries fourteen marks.**

## PART - A (10 x 3 = 30 Marks)

1. Explain NOT gate using NMOS.
2. What is the use of simulation?
3. Define library, entity and architecture in VHDL program.
4. Explain if statement.
5. Define half adder and full subtractor.
6. What is encoder?
7. Explain D Flip Flop
8. What do you mean clock'event AND clock=1?
9. Define PLD and state its advantages over fixed function ICs.
10. Compare PROM and PAL.

## PART - B (5 x 14 = 70 Marks)

11. (A) Implement the functions of $\overline{(A + B)\,C + D}$ and $\overline{A} + \overline{B}\,C$ using CMOS.

(OR)

(B) Explain placement and routing.

12. (A) Explain signal declaration and signal assignment statement.

(OR)

(B) Write the VHDL code for AND, NAND and EXOR gates.

13. (A) Explain full subtractor and write also its VHDL code.

(OR)

(B) Write the VHDL codes for 4 to 1 Multiplexer and 1 to 4 Demultiplexer.

14. (A) Develop the VHDL code for implementing TFF with and without reset input.

(OR)

(B) Develop the VHDL code for implementing Johnson counter.

15. (A) With the flowchart explain ASIC design flow.

(OR)

(B) Implement the function $F = \Sigma (1,5,7,11,15)$ in PLA.

M.Q.3

# MODEL QUESTION PAPER - II

Time : 3 Hrs  Max Marks : 100

Note : (i) Answel all the question from Part - A. Each question carries 3 marks.

(ii) Answer division (A) or (B) of each question in Part - B. Each question carries fourteen marks.

## PART - A (10 x 3 = 30 Marks)

1. Explain NOR gate using NMOS.
2. Define placement and routing.
3. Specify the various types of STD_LOGIC data types.
8. Explain case statement.
2. Define half subtractor and full adder.
6. Define Demultiplexer.
3. Explain T Flip Flop.
7. What is Johnson counter?
2. Define PROM and PLA.
8. Compare CPLD and FPGA.

## PART - B (5 x 14 = 70 Marks)

11. (A) Explain the different level of abstractions in VLSI design.

(OR)

(B) Explain stick diagram.

12 (A) Explain variable declaration and variable assignment statement.

(OR)

(B) Write the VHDL code for OR gate, NOR gate and NOT gates.

13. (A) Explain 4 bit arithmetic adder with its VHDL code.

(OR)

(B) With the logic diagram explain 4 bit arithmetic subtractor and write its VHDL code.

14. (A) Develop the VHDL code for implementing JKFF with and without reset input.

(OR)

(B) Develop the VHDL code for implementing Ring counter.

15. (A) Explain PROM and PLA.

(OR)

(B) Implement the function $F = \Sigma (1,5,7,11,13,14,15)$ in PROM.